Electronic Version
Stylesheet Version v1.1.1

CLOCK AND DATA RECOVERY CIRCUIT

Abstract

A clock and data recovery circuit generates a recovery and a reference clock corresponding to the input data and includes a phase shifter generating M discrete clocks at different phases, a data sampler generating a select signal according to the input data and the M discrete clocks, a primary phase selector outputting two consecutive discrete clocks and at least one interpolated clock with a phase between the phases of the two consecutive discrete clocks, a multiplexer selecting one of the two consecutive discrete clocks or the interpolated clock as a selected output clock, a phase detector receiving the selected output clock as the recovery clock and outputting an advanced calibration signal if the recovery clock leads or lags the input data, an advanced phase selector receiving the advanced calibration signal and transmitting the phase select signal to the multiplexer for adjusting the selected output clock and a primary calibration signal.